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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/070,035 | 07/03/2002 | Gilbert Wolrich | 10559-306US1 | 9914 |

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| EXAMINER | |
|---|---|
| PAN, DANIEL H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/070,035 | WOLRICH ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

2. Claim 1,19 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the element that constitute the information carrier (claim 1), or the medium (claim 19).

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1,19 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

4. As to claims 1, 19, Claims 1,19 are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 2, lines 6-13, the information carrier or the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., [microprocessor ]) and intangible embodiments ( e.g. [[Internet]). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,10,19, are rejected under 35 U.S.C. 102(b) as being anticipated by Aggarwal et al. (6,275,508)

As to claim 1, Aggarwal taught a system including at elast :

a) causing an executing instruction stream to branch (see the branch instruction in fig.12) to an instruction at an address specified in the instruction (branch address) if a state indicatina a current microenaine processina state (see the condition of microengine in col.4, lines 64-67, col.5, lines 1-9) of a specified state name [address field] is a specified value (see beanch address in col.10, lines 12-31).

6. As to claims 10, 19, Aggarwal taguht :

a) evaluating a value of a specifed state name (see thew selector of the conditinal branch in col.10, lines 20-31), the state name indicating a current microenaine processing state (see microengine in 4, lines 64-67, col.5, lines 1-22), and performing a branching operation based on the value of the specified state name being set or cleared (see also the microengine decision on 0 or 1 bit in col.6, lines 56-65).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa (5,724,563).

8. As to claims 1 , as to the language of "microengine" , the specfic structure of microengine is not being reflectd into the claim, therefore, Hasegawa's bracnh procesing is read as a microengine because it did hd the decisions on the driection of the instruciton procesing based on the state or condition (see also fig-s, and fig.lo, see also the implicit value Z or C encoded in opcode in Table 1 , col.l 1, lines 41-52, see also the teaching of Z and C flags set and reset in col.l 1, lines 14-40, lines 54-67, col.12, lines 1-5). Hasegawa taught a data processing system including a branch instruction that caused an execution of instruction stream to branch to an instruction at an address (x) specified in the instruction of a state incdicating curent microengine (microengine is read as the branch processing) state of a specified name was a specified value (see the branch instruction format in fig.z, see the value specified in the branch instruction field , see also fig-s, and fig.lo, see also the implicit value Z or C encoded in opcode in Table 1 , col.l 1, lines 41-52, see also the teaching of Z and C flags set and reset in col.l 1, lines 14-40, lines 54-67, col.12, lines 1-5).

9. As to claims 2,3, see the arithmetic flags set or reset in col.l 1, lines 19-32). As to the parallel processor , see the pipeline processor in fig.6).

10. register 8, instruction decoder 3 and execution unit 1 1).

11. As to claim 4, Hasegawa also included microengines (see fig.9 instruction

12. As to claim 6, ( see Branch 3, N in fig.5, see also the encoded branch opcode in Table 1 , for example, the first entry is (Branch on not equal Z). "Branch" being

"br inp state" "Z " being the state name, and the X being the label, the number 3 was an optional token.

13. As to claim 5, Hasegawa also specified the number of instructions top execute before performing the branch (see fig.5 Branch 3, X, see also fig.10).

14. As to claims 8,9 Hasegaga alos included performing the branch based on specified name (see branch on over flow set and branch on overflow clear in Table 1,see the flags set and reset in col.I 1, lines 14-35, see also the encoded flags in col.I, lines 42-52). As to the parallel processor , see the pipeline processor in col.5, lines 30-31).

15. As to claims 10,1 1 , 12, 19,20, Hasewaga also evaluated a value of a specified state name, and the state name indicating a current microenaine processing state and performing a branching operation based on the value of the specified state name being set or cleared (see Branch 3, N in fig.5, see also the encoded branch opcode in Table 1 , for example, the first entry is (Branch on not equal Z). "Branch" being "br inp state" "Z " being the state name, and the X being the label, the number 3 was an optional token.

16. As to claim 13, Hasegawa also included a label IxJ as a target filed (see the target address (x) in fig.5).

17. As to claims 14,15, Hasegawa also included an optional field for executing number of instructions before performing the branch (see fig.2 (23), see fig.5 Branch 3 X, see also fig.lo, see col.5, lines 55-67, see col.6, lines 24-32). As to the programmer

set token, Hasegawa 's instruction was also programmable (see the application program in col.l, lines 42-44).

18. As to claims 16, Hasegawa also included a register stack (see fig.l [register file] ; and a arithmetic unit (not qxplicitly shown as ALU, but it showed arithmetic calculations in col.l, lines 20-25, col.7, lines 44-52, see the adder in col.7, lines 52-56, fig.1, see counter section 4 in col.7, lines 8-26 for the increment and decrement, and comparison of the counter, see also the calculation section 7 in col.63-67, col.8, lines 1- 4, and see also the arithmetic result flags in coll 1 , lines 25-32). See also the branch on over flow set and branch on overflow clear in Table 1 for the feature of evaluating the specified value.

19. As to claim 17, Hasegawa did not explicitly show the additional microengine as claimed. However, Hasegawa , in the same patent, taught the parallel processor gpipeleine processor 200) could be implemented in two kinds of hardware having respective different instructions set pr use the same program code for both hardware (see col.13, lines 7-12). Therefore, additional hardware (or microengine ) was implemental be in Hasegawa.

20. As to claim 18, Hasegawa also included target field (x) (see fig.5).

21. Claim 1 is also additionally rejected under "102" over Dyer et al. (5,640,538) below :

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis'for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than on: year prior to the date of application for patent in the United States.

22. Claim 1 is rejected under 35 U.S.C. 102 (b) as being anticipated by Dyer et al. (5,640,538).

23. As to claim 1, Dyer taught a branch instruction that caused an execution of instruction stream to branch to an instruction at an address (80i) specified in the instruction of a state of a specified name ( e.g. branch type) was a specified value (spe branch type - 0,1 col.I 1, lines 8-10, see also the state of additional specified name in Table 1, see fig.8 for the branch instruction format).

16. The prior ad made of record and not relied upon is considered pedinent to applicant's disclosure.

a) Opalka et al. (6,259,699) is cited for the teahcing of the branch with microengine state (see col.16, lines 15-27).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***21 Century Strategic Plan***

/DANIEL H. PAN/
PRIMARY EXAMINER
GROUP